THAT WHICH IS CLAIMED IS:

1. An overvoltage protection circuit, comprising:

a pass transistor having first and second current carrying terminals electrically connected to an input signal line and an output signal line, respectively; and

a voltage clamping circuit comprising first and second diodes electrically connected in antiparallel between a power supply line and a gate of said pass transistor.

2. The circuit of Claim 1, wherein said first and second diodes comprise first and second NMOS transistors, respectively.

3. The circuit of Claim 2, wherein a source of the first NMOS transistor is electrically connected to a drain and gate of the second NMOS transistor and the gate of said pass transistor; and wherein a source of the second NMOS transistor is electrically connected to a drain and gate of the first NMOS transistor and the power supply line.

4. An overvoltage protection circuit, comprising:

a pass transistor having first and second current carrying terminals electrically connected to an input signal line and an output signal line, respectively; and

a voltage clamping circuit that is electrically connected to a power supply line and a gate of said pass transistor and dynamically clamps a capacitively bootstrapped voltage at a gate of said pass transistor within a first range so that magnitudes of all gate-to-source, gate-to-drain and drain-to-source voltages across said pass transistor do not exceed a voltage in excess of about Vdd when Vin is equal to about 2Vdd, where Vin equals a voltage of an input signal applied to the input signal line and Vdd equals a power supply voltage on the power supply line.

5. The circuit of Claim 4, wherein said voltage clamping circuit comprises a plurality of transistors; and wherein said voltage clamping circuit dynamically clamps a capacitively bootstrapped voltage at a gate of said pass transistor to within a first range so that magnitudes of all gate-to-source, gate-to-drain and drain-to-source voltages across said pass transistor and all the transistors within said voltage clamping circuit do not exceed a voltage in excess of about Vdd when Vin is equal to about 2Vdd.

6. The circuit of Claim 4, wherein said voltage clamping circuit comprises an NMOS transistor that is connected as a diode between a power supply voltage and the gate of said pass transistor; and wherein a maximum voltage within the first range is equal to about Vdd+Vth, where Vth equals a threshold voltage of said NMOS transistor.

7. The circuit of Claim 4, wherein said voltage clamping circuit comprises first and second diodes electrically connected in antiparallel between the power supply line and the gate of said pass transistor.

8. The circuit of Claim 7, wherein said first and second diodes comprise first and second NMOS transistors, respectively.

9. The circuit of Claim 8, wherein a source of the first NMOS transistor is electrically connected to a drain and gate of the second NMOS transistor and the gate of said pass transistor; and wherein a source of the second NMOS transistor is electrically connected to a drain and gate of the first NMOS transistor and the power supply line.

10. The circuit of Claim 9, wherein said voltage clamping circuit and said pass transistor collectively drive the output signal line with an output signal having maximum positive voltage equal to about Vdd for Vin greater than Vdd.

11. The circuit of Claim 9, wherein said voltage clamping circuit and said pass transistor collectively drive the output signal line with an output signal having a voltage that swings from a logic 0 reference level to a maximum positive voltage equal to about Vdd when Vin is switched from the logic 0 reference level to a positive voltage in a range between about Vdd and 2Vdd.

12. The circuit of Claim 10, wherein a minimum voltage within the first range is equal to about Vdd-Vth1, where Vth1 equals a threshold voltage of the first NMOS transistor.

13. An overvoltage protection circuit, comprising:

first and second pass transistors electrically connected in parallel between an input signal line and an output signal line;

a first power supply line electrically coupled to a gate of said second pass transistor;

a second power supply line; and

a voltage clamping circuit comprising first and second diodes electrically connected in antiparallel between said second power supply line and a gate of said first pass transistor.

14. The circuit of Claim 13, wherein said first and second diodes comprise first and second NMOS transistors, respectively.

15. The circuit of Claim 14, wherein a source of the first NMOS transistor is electrically connected to a drain and gate of the second NMOS transistor and the gate of said first pass transistor; and wherein a source of the second NMOS transistor is electrically connected to a drain and gate of the first NMOS transistor and said second power supply line.

16. The circuit of Claim 14, wherein said voltage clamping circuit clamps the gate of said first pass transistor at a maximum voltage of about $Vdd2+V_{TN2}$ in response to a positive input voltage transition in excess of about $V_{TN1}+V_{TN2}$ on the input signal line, where V_{TN1} and V_{TN2} are the threshold voltages of the first and second NMOS transistors, respectively.

17. The circuit of Claim 16, wherein said voltage clamping circuit clamps a voltage at the gate of said first pass transistor at a minimum voltage of about $Vdd2-V_{TN1}$ in response to application of a logic 0 signal to the input signal line, where V_{TN1} is a threshold voltage of the first NMOS transistor.

18. The circuit of Claim 16, wherein said first and second pass transistors comprise third and fourth NMOS transistors, respectively; and wherein V_{TN2} is about equal to a threshold voltage of the third NMOS transistor.

19. The circuit of Claim 13, wherein said first and second power supply lines are electrically connected together.

20. An overvoltage protection circuit, comprising:

a pass transistor having a first current carrying terminal electrically connected to an input signal line and a second current carrying terminal electrically connected to an output signal line; and

a voltage clamping circuit that is electrically connected to a gate electrode of said pass transistor, clamps a bootstrapped voltage at the gate electrode to a first voltage below a maximum voltage on the input signal line upon completion of a pull-up interval and clamps the bootstrapped voltage at the gate electrode to a second voltage that is higher than a minimum voltage on the input signal line upon completion of a pull-down interval.

21. The circuit of Claim 20, wherein the first voltage is greater than the second voltage.

22. The circuit of Claim 21, wherein said voltage clamping circuit comprises first and second diodes electrically connected in antiparallel between a power supply line and the gate electrode.